AMENDMENTS TO THE CLAIMS:

This listing of claims will replace all prior versions and listings of claims in the application:

1. (previously presented) A semiconductor device comprising:

a bit line extending in a first direction;

a plurality of transistors electrically connected to the bit line;

a plurality of first electrodes arranged in the first direction and electrically connected to the transistors;

a dielectric film covering upper and side surfaces of the first electrodes; and

a second electrode covering the dielectric film,

wherein the dielectric film, the second electrode, and each of the first electrodes form one of a plurality of capacitors,

wherein a width of the first electrode is smaller than a distance between adjacent first electrodes, and

wherein an angle defined by a line parallel to the first direction and a line parallel to a longitudinal direction of each of the first electrodes is larger than 0° and smaller than 90°.

2. (cancelled)

3. (previously presented) The device according to claim 1, wherein the angle is 45°.

4. (previously presented) The device according to claim 1, wherein the width of the first electrode is smaller than a minimum width of the bit line.

5. (previously presented) The device according to claim 1, wherein the width of the first electrode is smaller than a minimum width determined by lithography process.

6. (original) The device according to claim 1, wherein the width of the first electrode is smaller than a height of the first electrode.

7. (withdrawn) A method of manufacturing a semiconductor device, comprising:

forming a first film on a substrate including a bit line extending in a first direction and a plurality of transistors electrically connected to the bit line;

patterning the first film to form a plurality of trenches;

forming second films on side surfaces of the trenches to narrow the trenches;

forming, in the narrowed trenches, a plurality of first electrodes arranged in the first direction and electrically connected to the transistors;

removing the first film and the second films;

forming a dielectric film covering upper and side surfaces of the first electrodes; and

forming a second electrode covering the dielectric film.

8. (withdrawn) The method according to claim 7, wherein forming the second films on the side surfaces of the trenches is carried out using anisotropic etching.

9. (withdrawn) The method according to claim 7, wherein a width of the first electrode is smaller than a distance between adjacent first electrodes and smaller than the minimum value of design rule of the semiconductor device.

10. (withdrawn) A method of manufacturing a semiconductor device, comprising:

forming a first film on a substrate including a bit line extending in a first direction and a plurality of transistors electrically connected to the bit line;

patterning the first film to form a plurality of trenches;

forming second films made of conductive material on side surfaces of the trenches;

removing the first film;

patterning the second films to form a plurality of first electrodes arranged in the first direction and electrically connected to the transistors;

forming a dielectric film covering upper and side surfaces of the first electrodes; and

forming a second electrode covering the dielectric film.

11. (withdrawn) The method according to claim 10, wherein forming the second films on the side surfaces of the trenches is carried out using anisotropic etching.

12. (withdrawn) The method according to claim 10, wherein a width of the first electrode is smaller than a distance between adjacent first electrodes and smaller than the minimum value of design rule of the semiconductor device.

13. (previously presented) The device according to claim 1, wherein the semiconductor device is a semiconductor memory.

14. (previously presented) The device according to claim 1, wherein the semiconductor device is a random access memory.

15. (previously presented) The device according to claim 1, further comprising a plurality of plugs electrically connecting the first electrodes and the transistors.

16. (previously presented) The device according to claim 15, wherein the width of the first electrode is smaller than a diameter of the plug.

17. (previously presented) The device according to claim 15, wherein the plug includes a polysilicon plug portion and a metal plug portion formed on the polysilicon plug portion.

18. (previously presented) The device according to claim 15, further comprising a plurality of barrier films each provided between one of the first electrodes and one of the plugs.

19. (previously presented) The device according to claim 15, further comprising an isolation region and an element region surrounded by the isolation region, the element region having source and drain layers of the transistor.

20. (previously presented) The device according to claim 19, wherein the plug is connected to one of the source and drain layers.

21. (previously presented) The device according to claim 19, wherein the element region has a first portion extending in the first direction, and wherein the first electrode crosses the first portion.

22. (previously presented) The device according to claim 15, further comprising an interlayer dielectric film covering the transistor and surrounding the plug.

23. (previously presented) The device according to claim 22, further comprising a silicon nitride film provided between the dielectric film and the interlayer dielectric film.

24-33 (cancelled).